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Performance Evaluation of Irregular Modified Shuffle Multistage Interconnection Network

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Abstract—*Interconnection networks play significant role in various parallel processing applications. They specify the way in which the processors and the memory modules can be connected for efficient data transmission. Interconnection networks carry data between processors and to memory. Interconnections are build up of switching elements and links. Switches map a fixed number of inputs to outputs. Main considerations of designing interconnection networks are to provide fast, reliable, efficient, fault tolerant communication at reasonable cost among multiprocessors. Multistage Interconnection network is also an interconnection network in which switching elements are arranged in various stages. Therefore, the architecture of multistage interconnection networks is the vital design issue to achieve hike in performance parameters. In this paper, an improved irregular fault tolerant multistage interconnection network named Irregular Modified Shuffle Network (IMSN) is proposed and evaluated in terms of various performance parameters like bandwidth, probability of acceptance, processor utilization, processing power and throughput. Irregular networks imply unequal number of switching elements at various stages leading to low latency or delay. The results show that the proposed network named IMSN achieves valuable enhancement in performance parameters when compared with existing multistage interconnection networks like Improved Four Tree Network (IFTN), Modified Alpha Network (MALN) and New Irregular Augmented Shuffle Network (NIASN).*

1. INTRODUCTION

Parallel Processing offers a valuable way of decreasing execution time by implementing various events simultaneously in multiprocessor systems. Multistage Interconnection Networks (MINs) offer high bandwidth communication in multiprocessor systems. MINs have multiple stages of switches and switches are arranged in form of layers at each stage. Switches at each stage follow some pattern for interconnection allowing any input to be connected to any output. Based on interconnection pattern used in MINs, they are classified as blocking and non-blocking networks. In non-blocking networks, there exists a unique path between any source-destination pair and hence no path is obstructed. In blocking networks, due to availability of multiple paths some paths are blocked due to already established connection of some other source-destination pair. The pattern used for interconnection may be uniform or non-uniform based on which MINs are also categorized as regular or irregular networks. In regular networks, the number of switching elements is same at every stage and so is the path length and hence latency or delay is more. But in irregular networks the number of switching elements is not same at every stage and hence latency and path length is reduced. Also fault tolerance of regular networks is less because of lack of availability of paths as compared to irregular networks. Fault Tolerance is the ability to respond gracefully to various faults like switch fault in multiprocessor systems. MINs are cost effective means of providing multiple data paths between various functional units in multiprocessor systems. MINs offer proficient communication in data transmission.

In this paper, a new fault tolerant irregular multistage interconnection network named Irregular Modified Shuffle Network (IMSN) is proposed and analyzed. A comparison of IMSN is carried out with existing MINs like Improved Four Tree Network (IFTN) [9], New Irregular Augmented Shuffle Network (NIASN) [10] and Modified Alpha Network (MALN) [11] using various performance parameters like bandwidth, probability of acceptance, processor utilization, processing power, throughput and it has been observed that Irregular Modified Shuffle Network (IMSN) achieves great improvement in values of performance parameters over other existing MINs.

The paper is organized as follows. Section 2 describes proposed multistage interconnection network named IMSN. Section 3 describes performance evaluation parameters. Section 4 discusses the results in which the proposed network named IMSN is compared with existing networks like Improved Four Tree Network (IFTN) [9], New Irregular Augmented Shuffle Network (NIASN) [10] and Modified Alpha Network (MALN) [11] and it is followed by conclusions in Section 5.

2. PROPOSED MULTISTAGE INTERCONNECTION NETWORK (IMSN)

The structure of Irregular Modified Shuffle Network (IMSN) is shown in Fig. 1. IMSN is an irregular multistage

interconnection network of size NxN ($2^n x 2^n$) where N=16 as it has 16 sources and destinations (and $n=\log_2 N$). IMSN consists of $\log_2 N$ stages and as N=16, it has 4 stages. This network consists of 2^n multiplexers and 2^n demultiplexers of size 2x1 and 1x2 respectively. The first and last stage of the network consists of 2^{n-1} switching elements (SEs) and intermediate stages consist of less number of switching elements. The second stage of the network consists of 2^{n-3} switching elements and third stage contains 2^{n-2} switching elements. The first stage of the network has N/2 switches of size 3x3, the second stage of the network contains N/8 switches of size 5x5, the third stage of the network contains N/4 switches of size 2x8 and the last stage of the network has N/2 switches of size 5x2.

The SEs of first stage are linked to SEs of second and last stage, the SEs of second stage are connected to SEs of third stage, the SEs of third stage are connected to SEs of fourth stage as shown in Figure. Each source is connected to SEs of first stage using multiplexers and each destination is linked to SEs of last stage using demultiplexers. Two multiplexers are connected to each switching element at first stage and each switching element of last stage is connected to two demultiplexers. The SEs at first and second stage form auxiliary links to avail more paths to each source-destination pair. They can endure faults by following any alternate path available using auxiliary links. This network is double switch fault tolerant at first, third and fourth stage and single switch fault tolerant at second stage.

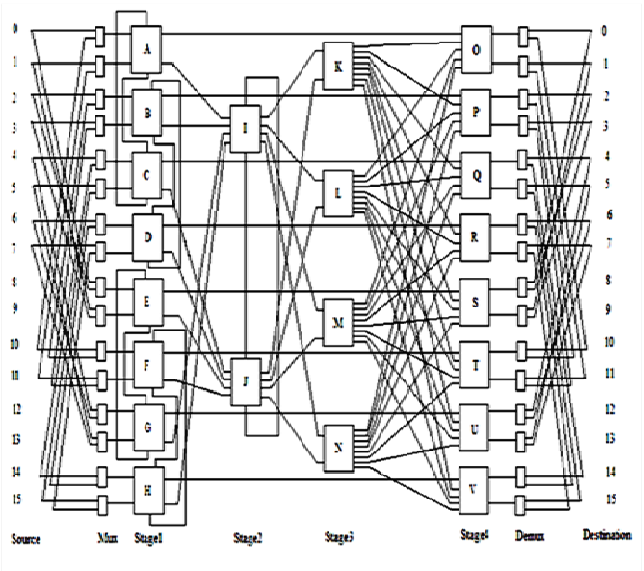

Fig. 1: Irregular Modified Shuffle Network (IMSN)

In this network, each source is connected to 3 SEs like source 4 is connected to switching elements C, G, H. Thus each source has 1 Primary SE like C to which it is directly connected and 2 alternate SEs like G and H to which it is connected indirectly. Similarly Primary and alternate switching elements of other sources can also be obtained. Therefore, in IMSN there are many alternate paths available for each source-destination pair.

Source, Mux, Stage 1, Stage 2, Stage 3, Stage 4, Demux, Destination of Irregular Modified Shuffle Network are shown in Fig. 1. Irregular Modified Shuffle Network (IMSN) being an irregular network supports various paths of different path lengths.

3. PERFORMANCE EVALUATION PARAMETERS

Irregular Modified Shuffle Network (IMSN) has been analyzed on the basis of following performance parameters.

3.1 Bandwidth (BW)

Bandwidth (BW) is the most common parameter used in analysis of multistage interconnection networks. It is defined as expected number of requests reaching the destination in any given cycle. In other words this parameter specifies number of requests which get matured. High Bandwidth is often desirable. If there are a^n sources and b^n destinations then Bandwidth will be [8]:

$BW = b^n p_n$

Here p_n is the request generation probability or load factor.

"Probability of one output getting the request from "a" inputs is: $1 - (1 - (p/b))^a$" [2].

Probability equations for NxN IMSN are:

$P[1]_{IMSN} = 1-(1-P[0]/3)^3$

$P[2]_{IMSN} = 1-(1-P[1]/5)^5$

$P[3]_{IMSN} = 1-(1-P[2]/8)^2$

$P[4]_{IMSN} = 1-\{(1-P[3])*(1-P[1]/2)\}^5$

Therefore, $BW_{IMSN} = (b^n * P[4]_{IMSN})$

Probability equations for NxN IFTN [9] are:

$P[1]_{IFTN} = 1-(1-P[0]/3)^3$

$P[2]_{IFTN} = 1-(1-P[1]/3)^3$

$P[3]_{IFTN} = 1-(1-P[2]/3)^3$

$P[4]_{IFTN} = 1-\{(1-P[3])*(1-P[1]/2)\}^2$

Therefore, $BW_{IFTN} = (b^n * P[4]_{IFTN})$

Probability equations for NxN NIASN [10] are:

$P[1]_{NIASN} = 1-(1-P[0]/3)^3$

$P[2]_{NIASN} = 1-(1-P[1]/3)^3$

$P[3]_{NIASN} = 1-\{(1-P[2])*(1-P[1]/2)\}^2$

Therefore, $BW_{NIASN} = (b^n * P[3]_{NIASN})$

Probability equations for NxN MALN [11] are:

$P[1]_{MALN} = 1-(1-P[0]/3)^3$

$P[2]_{MALN} = 1-(1-P[1]/6)^3$

$P[3]_{MALN} = 1-(1-P[2]/3)^3$

$P[4]_{MALN} = 1-\{(1-P[3])*(1-P[1]/2)\}^2$

Therefore, $BW_{MALN} = (b^n * P[4]_{MALN})$

The output of last stage will be used in obtaining the Bandwidth of the MIN.

3.2 Probability of Acceptance (PA)

The probability of acceptance is defined as the ratio of the expected number of successful requests to the expected number of requests submitted by the sources [10]. Therefore, it is the liability that the data packets sent form source side will be received by destination side without getting obstructed by other requests.

Formula for PA is:

$PA_{IMSN} = BW/a^n*p$

3.3 Processor Utilization (PU)

Processor Utilization is defined as percentage of time the processor is active doing internal computation without accessing the global memory [8].

Formula for PU is:

$PU_{IMSN} = BW/a^n*p*T$
T is the routing time between two nodes and node may be any source, destination or any SE.

3.4 Processing Power (PP)

It is defined as sum of processor utilization over the number of processors [10].

Formula for PP is:

$PP_{IMSN} = a^n*PU$

3.5 Throughput (TP)

Throughput means average number of cells delivered by a network per unit time. It is also defined as maximum number of traffic accepted by a network per unit time [3].

Formula for TP is:

$TP_{IMSN} = BW/a^n*T$

4. RESULTS

Based on the formulas discussed in Section 3 all the parameters are evaluated for IMSN, IFTN [9], NIASN [10], MALN [11] and the results are shown graphically. It is found that IMSN achieves better values than existing MINs like IFTN, NIASN and MALN.

Table 1: Performance Parameters of IMSN

Probability	Bandwidth	Probability of Acceptance	Processor Utilization	Processing Power	Throughput
0.1	4.888	3.055	1.222	19.552	0.122
0.2	8.131	2.541	1.016	16.262	0.203
0.3	10.328	2.151	0.860	13.766	0.258
0.4	11.836	1.849	0.739	11.836	0.295
0.5	12.888	1.611	0.644	10.310	0.322
0.6	13.641	1.421	0.568	9.094	0.341
0.7	14.179	1.266	0.506	8.102	0.354
0.8	14.572	1.138	0.455	7.286	0.364
0.9	14.864	1.032	0.412	6.604	0.371
1.0	15.08	0.942	0.377	6.032	0.377

The above table shows the values of performance parameters of IMSN. Performance parameters of IFTN [9], NIASN [10] and MALN [11] are also calculated and results are shown in following figures. Fig. 2 shows Bandwidth comparison of IMSN, IFTN, MALN, NIASN and it shows that results of IMSN are better than these existing networks. Fig. 3 shows Probability of Acceptance comparison of IMSN, IFTN, MALN, NIASN and results of IMSN are found to be better than these existing networks. Fig. 4 shows Processor Utilization comparison of IMSN, IFTN, MALN, NIASN and it shows that IMSN performs better than these existing networks. Fig. 5 shows Processing Power comparison of IMSN, IFTN, MALN, NIASN and results of IMSN are found to be better. Fig. 6 shows Throughput comparison of IMSN, IFTN, MALN, NIASN and IMSN achieves better values over these existing networks.

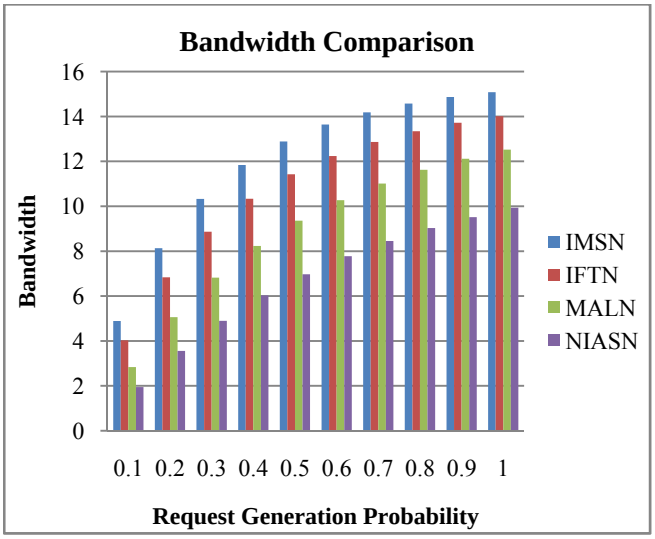

Fig. 2: Bandwidth Comparison

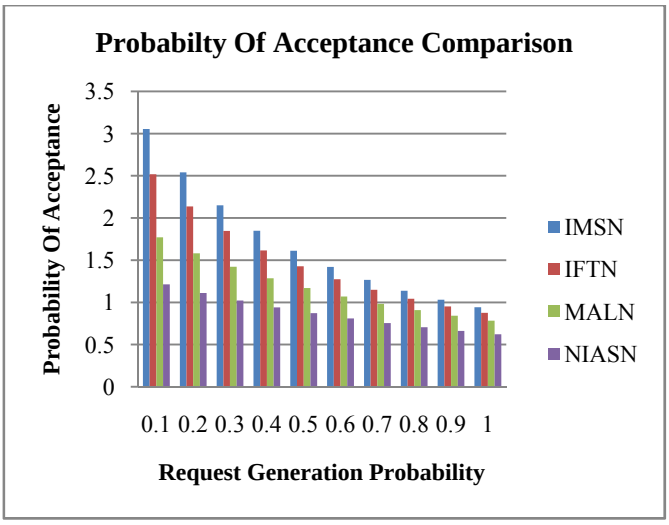

Fig. 3: Probability of Acceptance Comparison

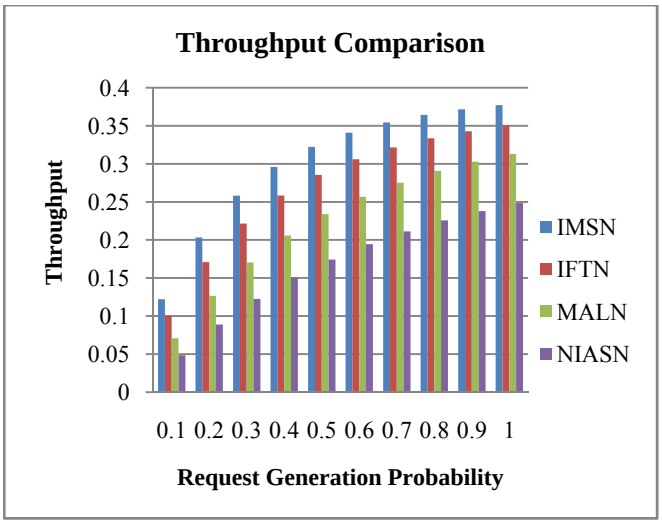

Fig. 6: Throughput Comparison

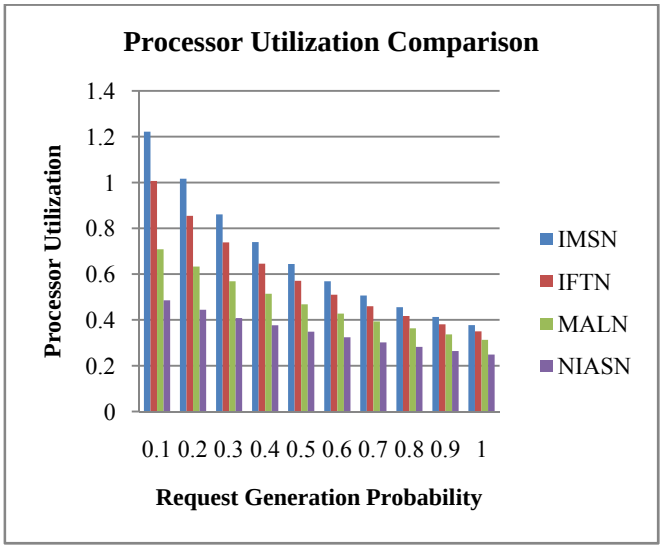

Fig. 4: Processor Utilization Comparison

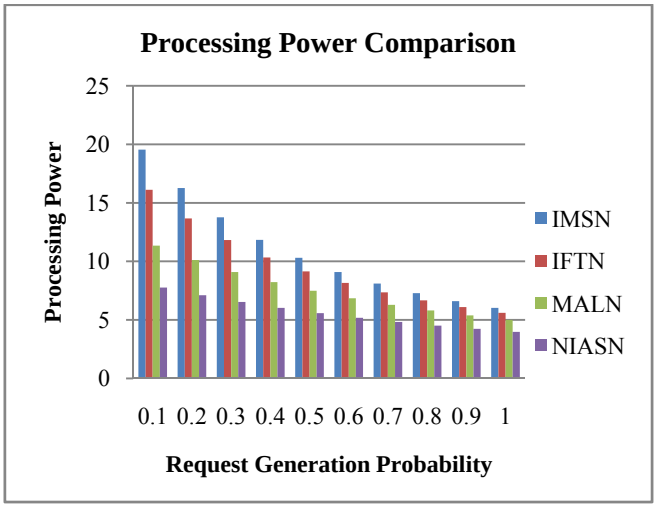

Fig. 5: Processing Power Comparison

5. CONCLUSION

In this research work, a new fault tolerant irregular multistage interconnection network named Irregular Modified Shuffle Network (IMSN) is proposed and analyzed. Comparison of new network named IMSN is made with various networks like IFTN [9], NIASN [10], MALN [11] in terms of various performance parameters. The results of all these multistage interconnection networks are shown graphically and it has been observed that newly proposed multistage interconnection network (IMSN) is found to better than other three networks. IMSN achieves valuable improvement in values of Bandwidth, Probability of Acceptance, Processor Utilization, Processing Power and Throughput.

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